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Gallium Arsenide as a Competitor to Silicon for High-speed Amplification and Switching*

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Abstract

A review is given of the physical and technological factors which affect the electrical behaviour of field-effect devices for high-speed applications. Ballistic electron transport is shown to lead to an electron transit time under the gate electrode which is shorter in GaAs than in Si field-effect transistors (FETs), providing a possible basis for exploitation of transport effects in high-speed devices. Some electrical characteristics of practical Si and GaAs field-effect structures are presented.

1. Introduction

In the continuing quest to reduce ever more complex signal processing functions to ever smaller dimensions, new materials, new techniques and new amplifying and switching device structures are coming to the forefront all the time. Much of what is done depends upon the efforts of the solid-state physicist in the first instance, yet it may take some years to realize the commercial potential of the work. It is not unknown, for example, for ideas to remain unexploited for the lack of suitable technology, or alternatively for hitherto unthought of phenomena to be revealed by the results of experiments made possible by new technology. Thus there exists, in the semiconductor device and integrated circuit business, a strong interdependence between solid-state physics, technology and device engineering. The evolution of interest in the semiconducting/semi-insulating III–V compound gallium arsenide has followed very much this kind of history, to the point where in some applications it has displaced the workhorse of the industry, silicon, almost completely.

Gallium arsenide has a number of very interesting properties. Its conduction band structure consists of a series of minima in the energy–wave vector (E–k) relationship (commonly termed 'valleys'), which depend upon the direction in reciprocal lattice space and whose energy separation makes possible the transfer of electrons from one (central or lower) valley to higher (or upper) valleys, as a result of energy acquired from an applied field (Sze 1969). The energy separation of the lower and upper valleys is less than the energy difference between the conduction and valence bands, so that the transferred electron effect occurs well before impact ionization across the bandgap. Since the curvature of the E–k relationship for the lower valleys is somewhat greater than it is for the upper valleys, the electron effective mass in the upper valleys is correspondingly larger and the drift velocity of electrons in the

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upper valleys is less than in the lower valleys (Carrol 1970). The velocity averaged over all electrons therefore drops as intervalley transfer takes place, leading to a velocity–field characteristic which exhibits a region of negative differential velocity quite unlike the saturating characteristic of Si (see Fig. 1). Of central importance is the fact that, were it not for the comparative inefficiency of the scattering mechanisms in the central valley in removing energy from the electrons present, the transferred electron effect would be nowhere near so obvious in GaAs as it is (Fawcett *et al.* 1970).

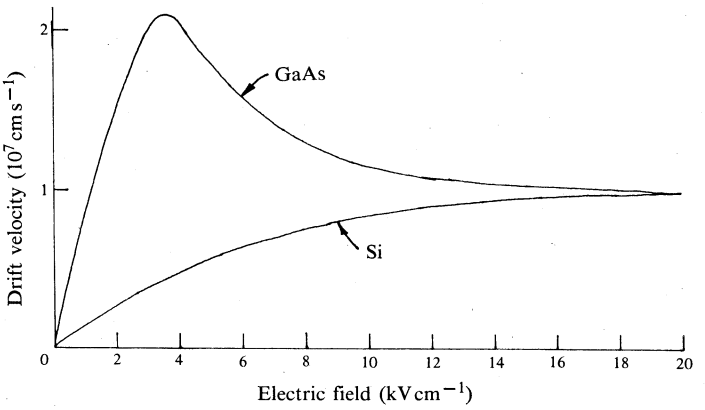

Fig. 1. Velocity–field characteristics for GaAs and Si.

A second helpful property of GaAs is that crystals of the material can be grown semi-insulating ($\sim 10^8\ \Omega$cm), thereby making available to the device engineer a nominally nonconducting substrate upon which useful devices can be built from doped layers, grown either by epitaxy or by annealed ion implantation (Rees 1980). The relevance of the semi-insulating condition is not what it might appear at first sight. Given that many of the device applications of GaAs involve energetic (or hot) electrons, it is frequently the case that carriers are scattered over the diffusion potential barrier into the substrate. The substrate is then not devoid of mobile charge carriers. Its importance is often that it is comparatively free of fixed ionic charge arising from impurity levels in the bandgap. This avoids the distortions to the electric field distribution in the total device which would arise from these charges and the undesirable influence of such field distortions on the overall current–voltage characteristics (Ladbrooke and Martin 1980). By way of comparison, Si is available in a high-resistivity form (not semi-insulating) with a resistivity of ~ 10 kΩcm (Mohr 1970).

For the past seven years, a study has been made at the University of New South Wales on the use of Si and GaAs in small FETs for high-speed amplification and switching. (By 'small' we mean that the principal dimension of the device in the direction of electron flow, in this case the gate length L, is comparable with the mean free path for scattering, i.e. $\lesssim 1\ \mu$m; see Fig. 2.)

A particularly important application of the basic device is the digital inverter shown in Fig. 3, which forms the prototype network for many large-scale integrated (LSI) and very large-scale integrated (VLSI) circuits. The inverter affords an excellent illustration of the role played by the physical properties of the materials and technological factors in deciding the switching speed of the entire circuit.

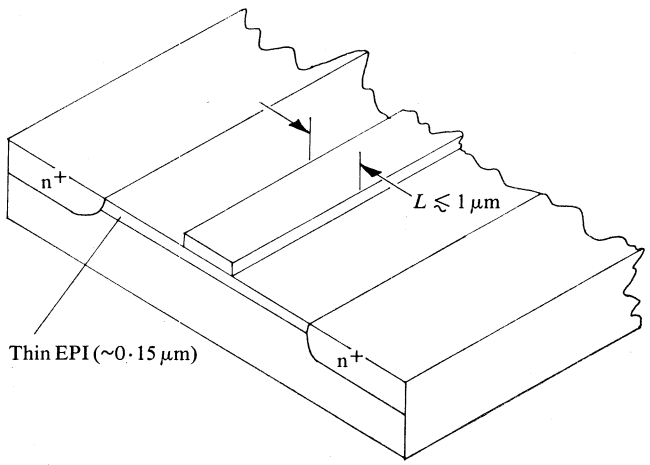

Fig. 2. Schematic diagram of a small depletion-mode FET, showing the epitaxial layer.

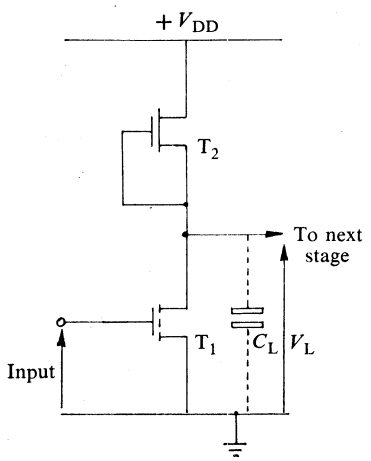

Fig. 3. Prototype network for a digital inverter circuit, showing the driver and load FETs T_1 and T_2 and the load capacitance C_L.

It may be shown that there is an advantage in making the load or pull-up FET T_2 a depletion-mode or 'normally on' device, so this type will be assumed henceforth. The driver T_1 will for present purposes be assumed to behave as an ideal switch which opens or closes in zero time: with these assumptions the speed of the circuit is determined by the rate at which T_2 can charge the load capacitance C_L when T_1 is turned off. Thus, when the channel current I_{DS} is independent of the time 't', the relationship governing the charge Q and voltage V_L across the capacitor C_L is

$$V_L = Q/C_L = (I_{DS}/C_L)t,$$

so that, if t_T is the time taken for V_L to reach the threshold for switching of the next stage (see Fig. 3), say $\frac{1}{2}V_{DD}$, then

$$t_T = \tfrac{1}{2} C_L V_{DD}/I_{DS}.$$

Substituting for I_{DS} from equation (A14) in the Appendix yields

$$t_T = \frac{C_L}{4C_G} \frac{V_{DD}}{(V_T V_{GC})^{\frac{1}{2}} - V_{GC}} \frac{L}{v}, \tag{1}$$

where from equation (A1) $V_{GC} = V_{BO}$ when the gate of the load FET is shorted to its source, as shown in Fig. 3. Although it involves a number of simplifications, the normalized form of this expression renders it particularly valuable for assessing the relative importance of key variables (Cooper 1981). For example, it is vital to minimize the extent to which the load capacitance C_L exceeds the FET input (or gate) capacitance C_G. Here C_L includes the output capacitance of the inverter, the metallization interconnect capacitance and the input capacitance of the next stage.

The factor of interest here is the ratio L/v, where L is the gate length and v the velocity with which the electrons drift from one side of the gate to the other. The ratio L/v thus represents the electron transit time under the gate. In equation (1), v is assumed constant for simplicity, whereas it is actually a function of position, and so it should therefore be viewed as some kind of average.

The shorter the transit time, the smaller is the circuit switching time. A proportional reduction in t_T should follow directly from either a decrease in L, an increase in v, or both. The minimum gate length L which can be achieved is dependent upon the lithographic process used during device fabrication, and is thus a technologically dependent factor. Increasing v is very much dependent upon the particular semiconductor in use.

Present-day technology makes possible the definition of gate control regions comparable with the mean free path for scattering in semiconductors, so that the velocity v is no longer totally limited by scattering processes, but is partly determined ballistically (Ruch 1972). Ballistic effects occur in GaAs for control electrode lengths of 1 μm or a little less, whereas in Si they occur for dimensions roughly an order of magnitude smaller. As a matter of principle, therefore, for 1 μm technology GaAs should offer a ballistic advantage over Si.

2. Physical Phenomena Governing Drift Velocity

When an electron enters the channel of a depletion-mode FET from the source electrode, it does so at the lattice temperature T_0. It is then accelerated by the electric fields in the channel, gaining momentum and energy from the fields as it progresses down the channel towards the drain. At the same time the electron loses momentum and energy to phonons or lattice waves. If the device is large enough (typically several microns) it eventually reaches a steady state where the energy gained per second equals the energy lost per second (and similarly for the crystal momentum). In submicron channel FETs this is not the case at all and the electron remains in a transient energy condition throughout (Ruch 1972; Huang and Ladbrooke 1977).

Several approaches are possible for determining the drift velocity v as a function of position as the electron passes under the gate. In decreasing order of complexity they are:

(1) Monte Carlo simulation of a complete device structure, including self-consistent solutions for the particle density and channel fields (Warriner 1977).

(2) Solution of the Boltzmann transport equation for the electron distribution function $f(\boldsymbol{k}, \boldsymbol{r}, t)$ (where we note that two distribution functions are required for

GaAs, one for the central valley and one for the equivalent upper valleys; see Conwell 1967).

(3) Solution of a set of moment equations, based upon some assumed form for the distribution function, expressing conservation of momentum and energy among the electrons constituting the distribution (Stratton 1962).

The third and simplest of these approaches, together with the assumption of a uniform channel field, suffices to examine the physics of electron velocity variation in the channel of a submicron gate FET (Huang and Ladbrooke 1977). By using the following single-electron equations, approximate solutions for $v(x)$ may be found:

$$m^* \, \mathrm{d}v/\mathrm{d}x + qv/\mu(T_e) = qE \qquad \text{(momentum)},$$

$$2\mu(T_e) Ek \, \mathrm{d}T_e/\mathrm{d}x + B(T_e) = q\mu(T_e) E^2 \qquad \text{(energy)},$$

where m^* is the electron effective mass, v is the drift velocity, q is the electron charge, E is the electric field strength (assumed independent of position x), μ is the electron mobility (as a function of electron temperature T_e), k is Boltzmann's constant and $B(T_e)$ is the average energy loss rate due to electron–lattice collisions.

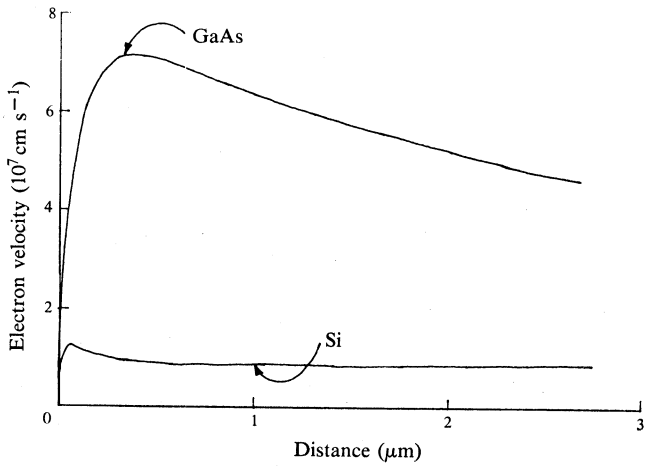

Fig. 4. Transient electron velocity as a function of distance from source contact for a uniform channel field $E = 20$ kV cm^{-1}.

Neglecting ionized-impurity and surface scattering also, we get the results for GaAs and Si given in Fig. 4 for a channel field of 20 kV cm^{-1}. In both cases the electron velocity overshoots the saturated drift velocity v_{sat} (the high-field value in Fig. 1) for some distance which is greater in GaAs than in Si. Although the end result is similar, the physical processes in the two materials which give rise to velocity overshoot are different. In Si, overshoot can be identified with the time taken, or equivalently the distance travelled, before the electron becomes hot (i.e. it is a 'cool' electron phenomenon). During this transient period the mobility is high compared with the value it eventually attains after 1 μm or so. The criterion for overshoot is simply that the carrier should be accelerated from rest while the mobility is still high. In other words, the momentum relaxation time $\tau_m \approx \mu_0 m^*/q$ should be smaller than the energy relaxation time $\tau_e \approx (\mu_0/v_{sat}^2) kT_0/q$. This is invariably true for all semiconducting materials, and more so for some than for others.

In the case of GaAs, the transport processes are more complex. The calculations which lead to Fig. 4 were based upon consideration of energy and momentum transport in the central valley only, with all electrons in the upper valley assumed to have a drift velocity of 10^7 cm s^{-1}. Velocity overshoot occurs in this material because, above an electron temperature of ≈ 1100 K, the increase in energy loss rate for central valley electrons with electron temperature is small and the carriers go on accelerating in the field until they acquire sufficient energy to transfer to the upper valleys (Maloney 1980). The distance for which velocity overshoot persists in Fig. 4 has been overestimated for GaAs by the neglect among other things of the difference in the density of states between the upper and lower valleys. More accurate results are available in the literature (Maloney and Frey 1977; Hill *et al.* 1977).

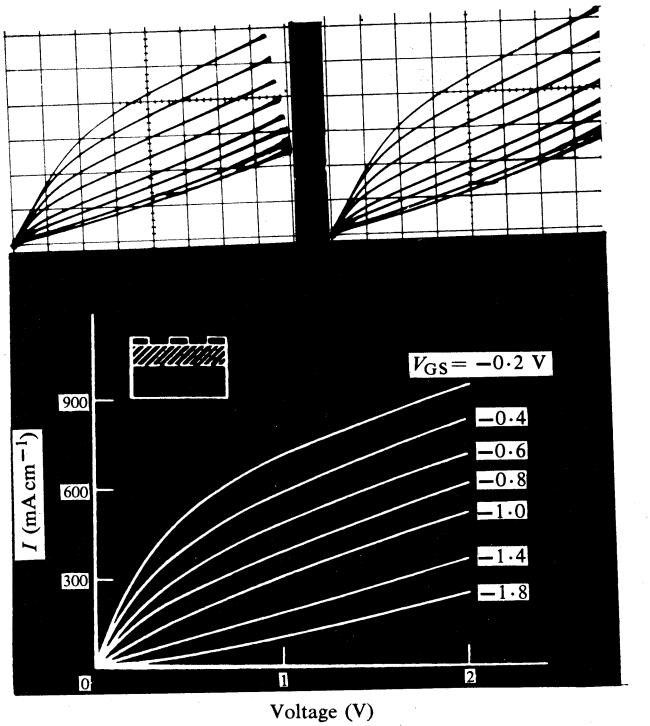

Fig. 5. *Above*: Drain characteristics of a doubly ion-implanted MOSFET with a channel length of ≈ 1 μm. (The two sets demonstrate uniformity between the two gates of a two gate structure.) *Below*: Computer simulation by Reiser and Wolf (1972) shown for comparison (for a 0·1 μm FET).

Despite the essentially crude nature of the foregoing calculations, they lead to the correct conclusion that, for gate lengths of $L \leqslant 1$ μm, a transit time L/v reduction of about five times should result for GaAs compared with Si. These calculations require consideration of the physical processes and the variation of electron temperature T_e with position x. The net result is an insight into the behaviour of the terminal characteristics of FET devices made from either material.

3. Practical Devices

Until recently, little emphasis seems to have been placed upon devising structures to make maximum use of the velocity overshoot phenomenon (Eastman *et al.* 1980; Hess 1981). Instead, there has been a comparatively straightforward development, in particular a reduction in size, of conventional metal-oxide semiconductor FETs (MOSFETs) and metal semiconductor FETs (MESFETs) (where the terminology relates to the method of constructing the gate or control electrode). In part this may be due to the complicating effect of many other factors, some of which are by now quite well quantified but others as yet barely recognized, which affect the electrical characteristics of a finished device. In such circumstances, only fairly general remarks can be made about the determinate nature of whatever processes may be involved, whether physical or technological in origin.

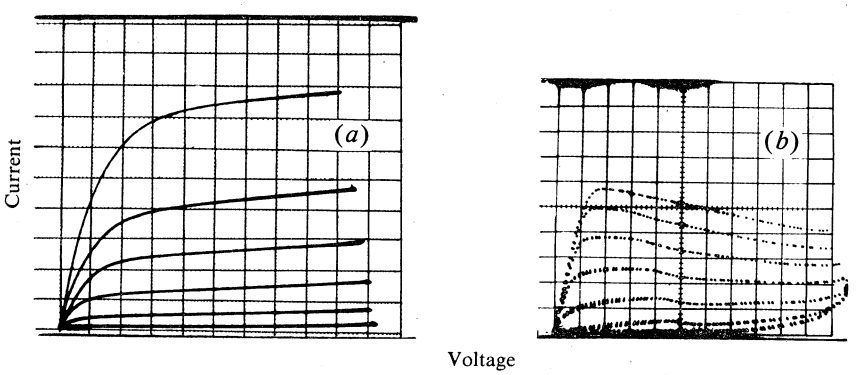

Fig. 6. Drain characteristics: (*a*) A silicon-on-sapphire FET; compared with Fig. 5 the current saturation is excellent. (*b*) A GaAs MESFET. In both cases the gate length is ≈ 1 μm.

In Fig. 5 we show the drain characteristics of doubly ion-implanted Si depletion-mode n-channel MOSFETs with a gate length of $\lesssim 1$ μm. Since the velocity overshoot illustrated in Fig. 4 can be expected to play only a minor part in determining the electrical characteristics, the behaviour shown in Fig. 5 must be dominated by other mechanisms. Computer simulations suggest that the Si FET can be adequately described at these gate lengths by a velocity–field characteristic, with energy and momentum relaxation processes neglected entirely (Reiser 1973). A major drawback with such Si transistors is the upward slope evident in the drain characteristics which, by a more elaborate analysis than that expressed by equation (1), may be shown to lead (undesirably) to a higher power dissipation per digital inverter stage for a given switching time t_T. Two phenomena must be considered in seeking an explanation for the high drain conductance. The first is the injection of energetic electrons from the channel into the substrate, where they give rise to a space-charge limited type of current flow (and then, in crude terms, the substrate behaves as a fixed resistor in parallel with the active FET; see Reiser 1970). The second is poor screening of the drain field from the channel, whereby the drain electrode acts as an inefficient gate inducing extra mobile charge in the channel with an attendant increase in channel (i.e. drain) current (Yamaguchi and Kodera 1977). Simulation suggests that the former is the dominant effect, in which event it should be possible to achieve well saturating drain characteristics by constructing the active device on a wide-bandgap

insulator, rather than on high-resistivity silicon. This possibility was confirmed by R. S. Huang at Cornell (personal communication, 1979), who used silicon-on-sapphire technology to achieve the results of Fig. 6*a*. It remains to be seen what acceptance silicon-on-sapphire gains in industry for submicron field-effect circuits.

In the absence of a proven stable oxide technology for GaAs (Colquhoun *et al.* 1978), the majority of the device and circuit work to date with this material has been in devices with metal–semiconductor (Schottky) barrier gates. The transport of electrons in such structures is similar in most respects to that in MOS transistors of the depletion type, so there is some basis for comparison of the two materials.

Fig. 6*b* shows the drain characteristics of a GaAs FET fabricated from an n-type layer grown epitaxially on a semi-insulating substrate. The gate length is again $\approx 1\ \mu$m. In sharp contrast to Si in Fig. 6*a*, there is a pronounced region of negative differential conductivity which is governed by the same physical processes giving rise to the velocity overshoot phenomenon. It may be shown, again in contrast to Si, that the power dissipated per digital stage is reduced by this effect for a given switching time t_T. In addition to a fivefold speed advantage, therefore, GaAs also promises smaller power dissipation, all other things being equal.

There is both theoretical (Warriner 1977; S. J. Beard, personal communication, 1978) and experimental (Eastman and Shur 1979; Tsironis 1980) evidence that in GaAs FETs, just as in Si FETs, energetic carriers pass into the substrate and contribute to the drain current. Unlike Si, however, such electrons do not necessarily lead to an upward sloping current–voltage relationship (and in fact the set of characteristics in Fig. 6*b* exhibits negative differential drain conductance over much of the current–voltage range). It is uncertain how widely the variation in the character of drain conductance is acknowledged. There is in any case no consensus as yet on the relative importance of space-charge limited current flow and low-level impact ionization in determining the substrate current (Eastman and Shur 1979; Tsironis 1980). In regions of the characteristics where the device fields are too small for impact ionization to be significant, one is ultimately left with the difficulty of explaining why the substrate current does not (in some practical cases at least) lead to positive drain conductance. It is possible that the intervalley transfer mechanism operates in the substrate as well as in the n-channel layer (indeed there is no reason why it should not), and that velocity reduction due to transfer outweighs the effect of increased electron numbers in the substrate as the field is increased, thereby preventing an increase in substrate current.

One very interesting practical observation to be made about some GaAs FET characteristics is that they apparently depend upon the speed of the bias pulse or sweep used to measure them (those in Fig. 6*b* were measured with a steady gate bias, but with 80 μs pulses applied to the drain; see Ladbrooke and Martin 1980). Our understanding of this dependence is poor at present, but work to date suggests that it may arise from levels of undetermined origin in the bandgap. The negative differential conductivity tends to disappear if the electrode voltages contain a large low-frequency component (i.e. bias), and the devices more readily exhibit breakdown effects. Both these points are of concern in large-signal applications.

4. Concluding Remarks

The technology of GaAs is sufficiently mature to allow the differences in electron transport properties of GaAs and Si to be exploited successfully in high-speed device

and circuit applications. Most of the effort to date has been concentrated on development of what might be referred to as 'traditional' FET structures and their integrated circuit derivatives, with comparatively little attention being paid to the possibilities for innovative devices to exploit, for example, the phenomenon of electron drift velocity overshoot.

Many questions remain to be answered. The importance of features of traditional FETs such as channel layer thickness and doping uniformity, doping profile, gate-edge uniformity, gate recesses, deep levels and substrate compensation are at best only qualitatively understood. The roles of surface scattering and surface charge have barely been touched upon.

Finally, advances made possible by technological innovation should be given the recognition they deserve. It is probably fair to say that the potential for developing new and ever smaller, ever faster devices, and hence ever more powerful signal and data processing circuits, depends intimately upon such advances in technology as ion implantation, molecular beam epitaxy and electron-beam microfabrication. With these techniques, the intellectual and commercial challenges extend well into the future.

Acknowledgment

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Appendix. Approximate Relationship for the Open-channel Current of a Depletion-mode FET in terms of Device Constants

For simplicity a Schottky FET structure is assumed: the argument is readily extended to MOS circuits by including the oxide capacitance of a depletion-mode MOSFET.

Consider a device of gate length L and active channel layer thickness d, with a gate–source voltage applied such that the width of the depletion layer under the gate at the source end of the channel is X (see Fig. 7). The following distinctions are drawn between the gate–channel potential V_{GC}, gate–source voltage V_{GS}, threshold potential V_T and pinch-off voltage V_P. Treating all potentials as positive, we have at the source end of the channel

$$V_{GC} = V_{GS} + V_{BO}, \tag{A1}$$

while at the drain end of the channel

$$V_T = V_P + V_{BO}, \tag{A2}$$

where V_{BO} is the built-in potential at the gate–channel contact.

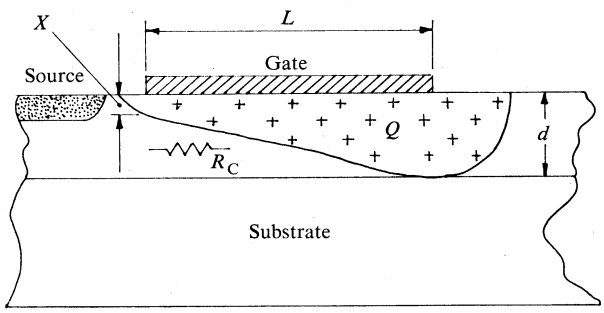

Fig. 7. Schematic diagram illustrating the depletion layer for an applied drain bias and a gate–source voltage held at zero.

By convention L is taken to be the dimension of the gate electrode in the direction of electron flow; the gate width W is the gate dimension in the transverse direction (i.e. into the page in Fig. 7).

With no applied gate or drain bias (i.e. $V_{GS} = 0$ and $V_{DS} = 0$), the channel will be uniformly depleted to a depth X, determined by the zero-bias barrier potential. Then the channel resistance is

$$R_{CO} = \frac{1}{N_D q\mu} \frac{L}{W(d-X)},$$

where N_D is the channel doping density, q the charge of an electron and μ the electron mobility in the channel (assumed constant).

With applied drain bias and the gate–source voltage held at zero, the depletion extends as shown in Fig. 7. The channel resistance R_C in this case is twice R_{CO}:

$$R_C = 2\frac{1}{N_D q\mu} \frac{L}{W(d-X)}. \tag{A3}$$

The total free charge in the channel with applied drain bias is

$$Q' = \tfrac{1}{2}L(d-X)WN_D q. \tag{A4}$$

Combining equations (A3) and (A4) we get

$$R_C = L^2/\mu Q'. \tag{A5}$$

Since the potential of the gate with respect to the channel at the drain end is V_T, and at the source end V_{GC}, the channel current is (from equations A1, A2 and A5)

$$I_{DS} \approx (V_T - V_{GC})/R_C = (V_P - V_{GS})Q'\mu/L^2. \tag{A6}$$

Taking $(V_P - V_{GS})/L$ as an estimate of the average electric field in the channel we have

$$\mu(V_P - V_{GS})/L = \mu E = v,$$

so that equation (A6) may be written

$$I_{DS} \approx Q'v/L. \tag{A7}$$

The next step is to replace Q' by an expression involving the gate capacitance C_G:

$$C_G = \frac{dQ}{dV_{GC}} = -\frac{dQ'}{dV_{GC}} = -\frac{dQ'/dX}{dV_{GC}/dX}, \tag{A8}$$

where

$$V_{GC} = \tfrac{1}{2}(q/\varepsilon)N_D X^2. \tag{A9}$$

From equations (A4) and (A9) we get

$$dQ'/dX = -\tfrac{1}{2}qN_D LW, \qquad dV_{GC}/dX = (q/\varepsilon)N_D X,$$

so that substituting into (A8) gives

$$C_G = \tfrac{1}{2}(\varepsilon/X)LW, \tag{A10}$$

which is one-half the value for a simple (isolated) rectifying contact.

Using equation (A9) we have

$$X = (2\varepsilon V_{GC}/qN_D)^{\frac{1}{2}}, \tag{A11}$$

and similarly

$$d = (2\varepsilon V_T/qN_D)^{\frac{1}{2}},$$

so that from (A4)

$$Q' = LW(\tfrac{1}{2}qN_D\varepsilon)^{\frac{1}{2}}(V_T^{\frac{1}{2}} - V_{GC}^{\frac{1}{2}}). \tag{A12}$$

Equations (A10)–(A12) then yield

$$C_G = Q'/2\{(V_T V_{GC})^{\frac{1}{2}} - V_{GC}\}. \tag{A13}$$

Eliminating Q' from equation (A7) by using (A13) gives finally

$$I_{DS} = 2C_G\{(V_T V_{GC})^{\frac{1}{2}} - V_{GC}\}v/L. \tag{A14}$$

This is the particular form required for the analysis in Section 1. It should be noted that (A14) does not give the voltage dependence of I_{DS} explicitly because C_G is a function of V_{GC}. Such an explicit relationship is available from equations (A6) or (A7) and (A12).

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